



PATENT  
Docket No. SPLX.P0072

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In the application of:

Steven Teig

Serial No.: 10/066,060

Filing Date: 1/31/2002

For: METHOD AND APPARATUS FOR  
ROUTING A SET OF NETS

Examiner: Phallaka Kik

Group Art Unit: 2825

**INFORMATION DISCLOSURE  
STATEMENT UNDER 37 C.F.R. § 1.97**

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This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to

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Dated: August 24, 2004

Respectfully submitted,

By: \_\_\_\_\_

**Mani Adeli**

Registration No. 39,585

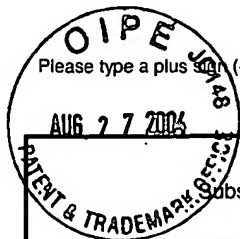
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<b>Substitute for form 1449A/PTO</b> <b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b>  (use as many sheets as necessary)				<b>Complete if Known</b>	
				Application Number	10/066,060
				Filing Date	1/31/2002
				First Named Inventor	Steven Teig
				Group Art Unit	2825
				Examiner Name	Phallaka Kik
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FOREIGN PATENT DOCUMENTS								
Examiner* Initials	Cite No. <sup>1</sup>	Foreign Patent Document			Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T <sup>6</sup>
		Office <sup>3</sup>	Number <sup>4</sup>	Kind Code (if known) <sup>5</sup>				
	1.	JP	02-262354		10-25-1990	Kuribayashi, Mototaka		

NON PATENT LITERATURE DOCUMENTS				
Examiner* Initials	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>6</sup>	
	2.	CHO J.D., Wiring Space and Length Estimation in Two-Dimensional Arrays, May 2000, Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on, VOL. 19, Iss. 5, pp. 612-615.		
	3.	CONG J. et al., DUNE – A Multilayer Gridless Routing System, May 2001, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 20, iss. 5, pp. 633-647.		
	4.	DION J. et al., Contour: A Tile-based Gridless Router, March 1995, Digital Western Research Laboratory, research Report 95-3, pp. 1-22.		
	5.	JUTTNER et al., "Lagrange Relaxation Based Method for the QoS Routing Problem, IEEE, Apr. 26, 2001, pp 259-268.		
	6.	SCHULZ U., Hierarchical Physical Design System, CompEuro '89, VLSI and Computer Peripherals. VLSI and Microelectronic Applications in Intelligent Peripherals and their Interconnection Networks. Proceedings, 8-12 May 1989, pp. 5/20 - 5/24.		
	7.	TSENG H-P. et al., A Gridless Multilayer Router for Standard Cell Circuits Using CTM Cells, Oct. 1999, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol 18, iss. 10, pp. 1462-1479.		

Examiner Signature	Date Considered
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\* EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. <sup>1</sup> Applicant's unique citation designation number (optional). <sup>2</sup> See Kinds Codes of USPTO Patent Documents at [www.uspto.gov](http://www.uspto.gov) or MPEP 901.04. <sup>3</sup> Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). <sup>4</sup> For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. <sup>5</sup> Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. <sup>6</sup> Applicant is to place a check mark here if English language Translation is attached.

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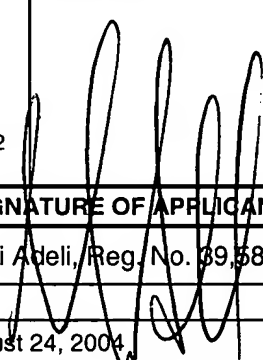
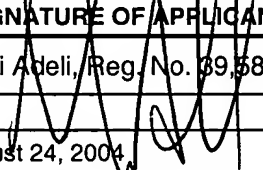


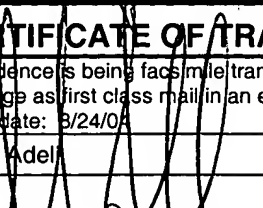
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<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/066,060
	Filing Date	1/31/2002
	First Named Inventor	Steven Teig
	Group Art Unit	2825
	Examiner Name	Phallaka Kik
Total Number of Pages in This Submission	Attorney Docket Number	SPLX.P0072

Enclosures (Check all that apply)		
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